REMARKS

Status of the Claims

Claims 22-37 are pending, with Claims 22, 38, and 39 being independent.

Applicant respectfully requests the Examiner to reconsider and withdraw the outstanding rejections in view of the following remarks.

Form PTO-892

Applicant respectfully requests correction of the Form PTO-892 attached to the Office Action mailed on September 9, 2004, which incorrectly lists U.S. Patent No. 5,922,673 to Gluckman et al., instead of U.S. Patent No. 5,292,673 to Shinriki et al.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 22-40 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,091,763 ("Sanchez") and further in view of U.S. Patent No. 5,880,508 ("Wu") and U.S. Patent No. 5,322,809 ("Moslehi"). Applicant respectfully disagrees with the rejection; therefore, this rejection is traversed.

Sanchez is cited as allegedly disclosing an interfacial layer on a silicon semiconductor substrate; a gate electrode of an electrically conductive material; a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; source and drain regions that are adjacent the gate electrode; a pair of spacers formed

adjacent to the gate electrode; and a pair of second spacers that are adjacent to the first spacers and formed on the lightly doped regions.

Wu is cited as disclosing a high dielectric constant layer, that comprises a material of Ta_2O_5, wherein the interfacial layer comprises silicon nitride or silicon oxynitride and a barrier layer between the gate electrode and the high dielectric constant layer. The Office Action alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Wu with Sanchez, because the high dielectric constant layer provides for agate insulator layer that reduces hot carrier effect and the barrier layer helps to provide better adhesion between the high dielectric constant layer and the gate.

Moslehi is cited as disclosing a planar interlayer insulator and silicide on the source and drain regions. The Office Action further alleges that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Moslehi with Sanchez, because the silicide on the source and drain provides for a lower resistivity for better electrical conduction for metal contact and the planar insulator keeps topography level so preceding layers can be uniform.

The Office Action additionally alleges that as Applicant has not disclosed that when used in a device, the claimed various high dielectric compositions provide unique or different results from the Ta_2O_5 material, listed in the group, disclosed by Wu, the claimed materials that are not shown by the prior art of record do not provide patentable distinction from the materials given in the prior art of record. Thus, the rejection is fatally defective since the Office Action admits that the prior art fails to suggest all of the claim limitations.

Sanchez discloses a high speed submicron transistor which exhibits a high immunity to hot electron degradation and is viable for VLSI manufacturing. (Abstract). Sanchez discloses a MOS transistor which shows good reliability and performance with channel lengths down to 0.3 μm for 5 v operation. (Column 3, Lines 34-37).

Wu discloses a transistor formed on a semi-conductor substrate, where the transistor includes a gate dielectric layer formed on the semi-conductor substrate. (Abstract).

Moslehi discloses a self-aligned silicide process that enables different silicide thicknesses for polysilicon gates and source/drain junction regions. (Abstract).

In contrast, Claim 22 recites an MOS transistor formed on a semiconductor substrate of a first conductivity type comprising: (a) an interfacial layer formed on the substrate; (b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source

and drain regions of a second conductivity type; and (f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

Claim 38 recites an MOS transistor formed on a semiconductor substrate of a first conductivity type comprising: (a) an interfacial layer formed on the substrate, wherein the interfacial layer comprises silicon nitride; (b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of a second conductivity type; and (f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

Claim 39 recites an MOS transistor formed on a semiconductor substrate of a first conductivity type comprising: (a) an interfacial layer formed on the substrate, wherein the interfacial layer comprises silicon oxynitride; (b) a high dielectric constant layer formed on the interfacial layer that comprises a material that is selected from the group consisting of

Ta_2O_5, $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, and mixtures thereof wherein the interfacial layer separates the high dielectric constant layer from the substrate; (c) a gate electrode having a width of less than 0.3 micron covering the high dielectric constant layer; (d) first and second lightly doped regions of a second conductivity type disposed on respective areas of the substrate surface; (e) a source and drain regions of a second conductivity type; and (f) a pair of spacers formed adjacent to the gate electrode and formed on the high dielectric constant layer.

Basic Requirements of a *Prima Facie* Case of Obviousness

As explained in MPEP § 2143, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Applicant respectfully submits that Sanchez further in view of Wu and Moslehi does not teach or suggest all the claim limitations. In particular, Applicant respectfully submits

that the combination of Sanchez, Wu, and Moslehi is not suggestive of the combination of features recited in Claims 22-40, which includes a gate electrode having a width of less than 0.3 micron. In citing Sanchez as disclosing a gate electrode having a width of less than 0.3 micron, the Office Action references column 3, lines 34-37 of Sanchez, which actually discloses channel lengths down to 0.3 μm, not a gate electrode width of less than 0.3 microns.

As the prior art references when combined do not teach or suggest all the claim limitations, a *prima facie* case of obviousness has not been established. Accordingly, withdrawal of the rejection under 35 U.S.C. § 103(a) is respectfully requested.

Legal Concept of *Prima Facie* Obviousness

As explained in MPEP § 2142, "The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness."

As noted above, the Office Action concedes that none of Sanchez, Wu, or Moslehi discloses "the various high dielectric compositions" presently claimed. As such, the Office Action fails to set forth a *prima facie* case of obviousness. Given the lack of a *prima facie* case of obviousness, there is no justification for the following position taken in the Office Action:

However, applicant does not disclose that these materials will provide unique or different results, when used in a device, from the Ta_2O_5 material, listed in the group, disclosed by Wu. Therefore, the other materials that are not shown by the prior arts of record are considered to be equivalent and a matter of design choice. No criticality has been placed on using one material over the other and therefore do not provide patentable distinction from the materials given in the prior arts of record.

Applicant respectfully submits that as the examiner has not met the initial burden of factually supporting any *prima facie* conclusion of obviousness, the applicant is under no obligation to submit evidence of nonobviousness.

Conclusion

For the reasons noted above, the art of record does not disclose or suggest the inventive concept of the presently claimed invention as defined by the claims.

In view of the foregoing remarks, reconsideration of the claims and allowance of the subject application is earnestly solicited. The Examiner is invited to contact the undersigned at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted,

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